Letter
Design of a Reconfigurable Acoustic Modem for Underwater Sensor Networks

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SUMMARY  Design of acoustic modem becomes increasingly important in underwater sensor networks' development. This paper presents the design of a reconfigurable acoustic modem, by defining modulation and demodulation as reconfigurable modules, the proposed modem changes its modulation scheme and data rate to provide reliable and energy efficient communication. The digital system, responsible for signal processing and control, is implemented on Xilinx Virtex5 FPGA. Hardware and software co-verification shows that the modem works correctly and can self-configure to BFSK and BPSK mode. Partial reconfiguration design method improves flexibility of algorithm design, and slice, LUT, register, DSP, RAMB are saved by 17%, 25%, 22%, 25%, 25% respectively.

key words: acoustic modem, partial reconfiguration, underwater sensor networks

1. Introduction

There is a growing interest in building underwater sensor networks for oceanographic applications such as marine exploration, environmental monitoring, mine detection and coastal surveillance. Underwater networks depend on physical layer acoustic modem for data collection, transmission and reception. And the preferred mode of wireless communication is based on acoustic signal. Unfortunately, due to the low propagation speed of sound wave approximately 1500 m/s and the complexity of underwater environment, the underwater acoustic communication is characterized with limited bandwidth, long propagation delay, large and variable multipath delay spread and Doppler shift [1]. This severe channel condition poses great challenge for underwater acoustic modem design.

Various work has been done on acoustic modem design. Acoustic modems with DSSS, ASK modulation scheme communicating at data rate of 133, 100 were proposed in [2], [3]. To ensure reliable communication, these modems are designed considering the worst-case channel assumptions. Unfortunately this often leads to communicating at lower data rate than practically possible and scarce bandwidth resources are wasted. Moreover, due to the high transmitting power of acoustic modems, lower data rate results in substantial increase in the energy consumed per bit.

Since acoustic modems are battery powered, energy efficient communication is crucial to enlarge the underwater networks' lifetime. Some researchers recognize that communication performance underwater depends on the deployment environment, thus modems with adaptive features have been proposed. WHOI micromodem [4] has two operation mode: low data rate FH-FSK mode and high power variable rate PSK mode. Y. Tao et al. proposed a dual-mode acoustic modem which switches between 4FSK and DBPSK [5]. Y. Li et al. proposed an acoustic modem with various modulation schemes namely QPSK, DSSS and OFDM [6]. However, these modems require the user to set communication parameters prior to deployment and they are not designed to adapt to variable channels after the network is deployed.

This paper proposes a reconfigurable acoustic modem for underwater sensor networks. The modem changes its modulation scheme and data rate according to the real-time channel conditions to provide reliable and energy efficient communication. Although most of the existing research modems are implemented on software or DSP for simplicity, we choose FPGA as the hardware platform for signal processing and control due to its lower power and faster processing speed [7]. By exploring partial reconfiguration (PR) design method, the proposed modem configures itself to the appropriate modulation scheme by on-the-fly programming. Experiment results on Xilinx Virtex5 FPGA show that the reconfigurable modem works correctly and can switch between BFSK and BPSK mode. Partial reconfiguration design improves flexibility of algorithm design and saves resource utilization of the modem.

2. Reconfigurable Acoustic Modem Design

2.1 Modem Architecture

Underwater acoustic modems work in half-duplex mode and consist of three fundamental components as shown in Fig. 1: transducer, analog transceiver and digital system.

The transducer converts analog electrical signal to acoustic wave and vice versa. The analog transceiver consists of a transmitter which amplifies signal in transmitting mode and a receiver which filters the signal in receiving mode. The digital system is responsible for signal processing and control, and it is the key part of the reconfigurable modem. Design of the transducer and the analog transceiver is described in [8]. In this paper, we mainly focus on the design and implementation of the digital system.
2.2 Digital System Design

The digital system is an embedded system and configures itself to the appropriate modulation scheme and date rate based on estimated channel SNR. It mainly includes four modules: channel estimation, symbol synchronization, controller, modulation and demodulation.

Channel estimation is an important part of the reconfigurable modem. We selected chirp signal for channel estimation due to its good autocorrelation property. By sending a chirp signal, underwater channel parameters including SNR, Doppler shift and multipath delay are measured [9].

Symbol synchronization is important to any wireless communication. It is critical that the receiver correctly determines the beginning of the incoming data packet for demodulation. We perform synchronization by correlating the received signal with known preambles namely Gold code and a chirp signal. Sea test results in Pacific Ocean showed chirp was able to successfully synchronize 100% while Gold code could only synchronize about 70%. Therefore, chirp signal is used for synchronization in the proposed modem.

The proposed reconfigurable modem changes its modulation scheme according to channel SNR to provide efficient communication, but at a certain time only one specific modulation scheme is needed for communication. This characteristic inspires us to explore the PR feature of FPGA. PR further enhances reconfigurability and flexibility of FPGA by allowing modification of a portion of the design on-the-fly without interrupting other parts. Therefore, modulation and demodulation are defined as reconfigurable modules (RM) and their function is changed by on-site programming. The modem can switch among any modulation scheme that is suitable for underwater channel and we studied BFSK and BPSK in this paper. BFSK is used to communicate when channel SNR is below 10 and BPSK is used for SNR above 10. The signal parameters are listed in Table 1.

FSK is a fairly simple and widely used modulation scheme in underwater communication due to its intrinsic robustness to time and frequency spreading. In BFSK modulator, information is transmitted by discrete frequency change of the carrier wave. The block diagram of BFSK demodulator is shown in Fig. 2. The received signal is first down converted to baseband then non-coherent energy detection method is used for demodulation. Phase coherent modulation techniques were demonstrated to be a viable way of achieving high-speed data transmission over many underwater channels [10]. In BPSK modulator, the carrier’s phase is 0 or 180 degree for digital data of 0 or 1 respectively. In BPSK demodulator, costas loop is used for coherent demodulation and carrier recovery as shown in Fig. 3. NCO adjusts local carrier’s frequency based on the detected phase error, and LPF output of I-branch is the demodulation result.

The controller orchestrates the digital system and FPGA soft processor Microblaze is instantiated as controller. Based on channel SNR, Microblaze configures the RM to BFSK or BPSK mode and sets the data rate. During the reconfiguration, Microblaze first loads the partial bit-stream file of the appropriate modulation scheme stored on system advanced configuration environment (System ACE) CF memory to FPGA configuration memory. Then internal configuration access port (ICAP) enables Microblaze to read the configuration memory at run time to program the RM, thus circuit structure and functionality of RM are modified during the digital system’s operation.

By exploring PR design method, the proposed modem change its modulation scheme by on-site programming and it switches among different modulation schemes without implement all of them on FPGA. Therefore, resources are expected to be saved.

### Table 1 BFSK BPSK signal parameters.

<table>
<thead>
<tr>
<th>Modulation</th>
<th>BFSK</th>
<th>BPSK</th>
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<tbody>
<tr>
<td>Space frequency</td>
<td>36 kHz</td>
<td>35 kHz</td>
</tr>
<tr>
<td>Mark frequency</td>
<td>37 kHz</td>
<td>35 kHz</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>35 kHz</td>
<td>35 kHz</td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>192 kHz</td>
<td>192 kHz</td>
</tr>
<tr>
<td>Data rate</td>
<td>200 bps</td>
<td>1000 bps</td>
</tr>
</tbody>
</table>

### Fig. 2 BFSK demodulator block diagram.

### Fig. 3 BPSK demodulator block diagram.
3. Experiment and Results

To evaluate the performance of the reconfigurable acoustic modem, we implemented its digital system on Xilinx Virtex5 FPGA. Ideally, the proposed modem changes its modulation scheme based on channel SNR, since we have not finished integrating the transducer and analog transceiver, in the experiment the modulation and demodulation modules were connected directly and Hyperterminal was used to enter command to set the modulation scheme.

We followed the PR design flow and built project in Xilinx PlanAhead development environment to generate the system ACE file and partial bitstream files of the reconfigurable modules and then save them on CF memory. ACE file is a data compression archive file and is used to configure FPGA device, initialize BRAM, and boot up Microblaze.

When the FPGA board was powered on, system ACE file was firstly loaded to initialize the system hardware and software, and init_done was printed on Hyperterminal. We then typed command f in Hyperterminal, Microblaze loaded fsk.bit and configured the modem to BFSK mode, and sent 60 bits of data to modulation module. When demodulation was finished, an interrupt signal was generated and Microblaze read the demodulation result. Alternatively, we typed p to configure the modem to BPSK mode. We used Xilinx Chipscope Analyzer to observe the main signal in the digital system, and the waveform is shown in Fig. 4. As we can see, the modulation data $T_x.data_{out}$ and the demodulated results $R_x.data_{out}$ sending back to Microblaze are the same in both BFSK and BPSK mode. The results demonstrate that the reconfigurable modem works correctly, and it can be configured to BFSK or BPSK mode.

Resource utilization of the digital system is shown in Table 2. When defining PR region on FPGA, it should comprise enough resources to accommodate all the partial bitstream files. Since BFSK occupies more logic than BPSK, the resource of PR region is defined the same as BFSK. Compared to traditional FPGA design method, the proposed reconfigurable modem achieves modulation scheme adaption by loading its corresponding bitstream files, and it does not implement all the modulation schemes on FPGA, therefore resources are saved. In BFSK and BPSK mode, slice, LUT, registers, DSP, RAMB are appropriately saved by 17%, 25%, 22%, 25%, 25% respectively.

4. Conclusion and Future Work

In this paper, a reconfigurable acoustic modem for underwater sensor networks is developed. Due to the spatially and temporarily variable channel condition, the proposed modem adapts its modulation scheme and data rate by on-site programming to provide reliable and energy efficient communication. PR design method improves design flexibility and the reconfigurable modem can extend to other modulation schemes like DSSS, OFDM without increasing hardware resource. Future work includes integrating each part of the modem in a housing and performing sea test.

References